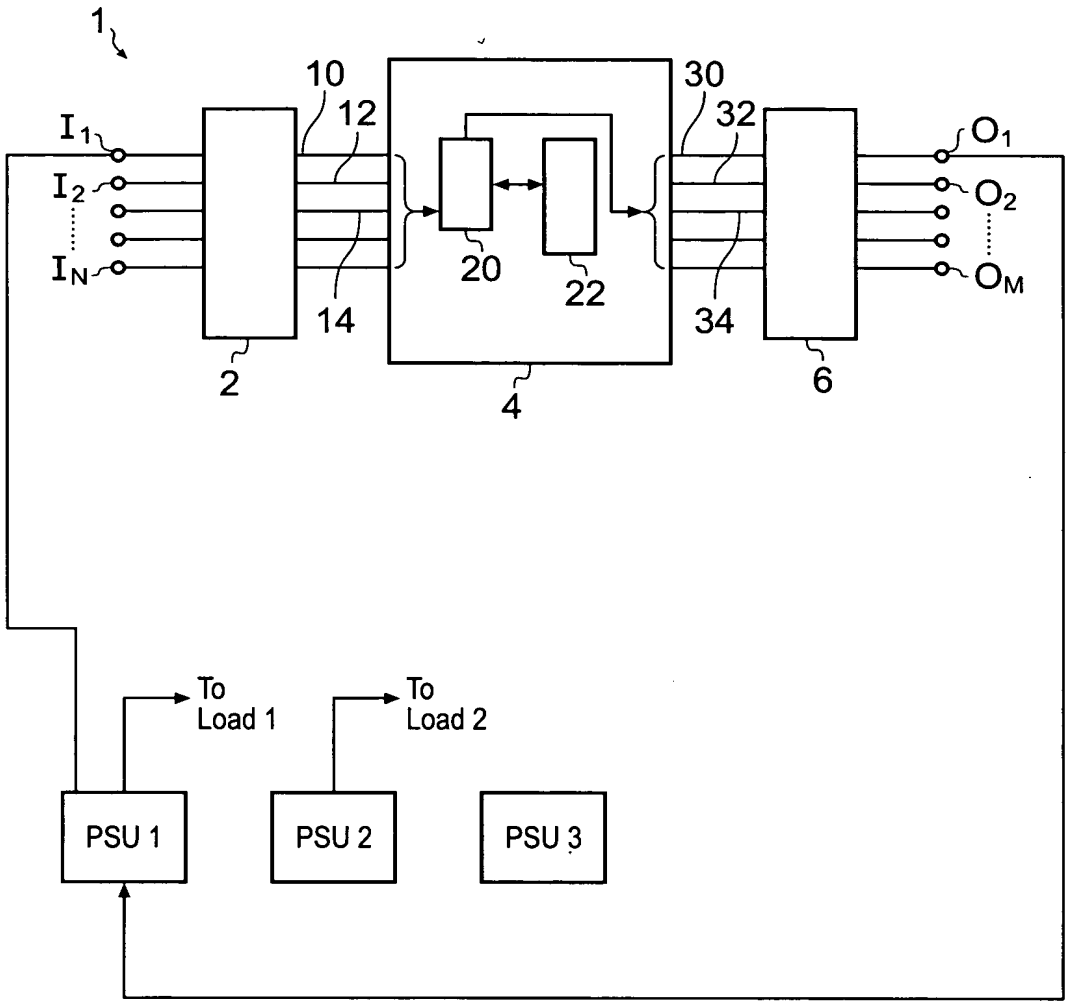
1
10
12
30
32
I_1
I_2
I_N
O_1
O_2
O_M
20
22
14
34
2
4
6
To
Load 1
To
Load 2
PSU 1
PSU 2
PSU 3

Fig. 1

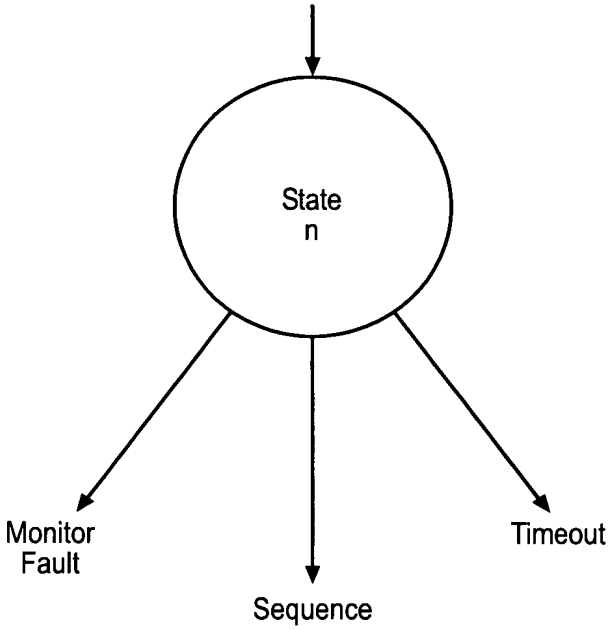

Fig. 2

PDO Outputs	IDLE1	IDLE2	EN3V3	EN2V5	DIS3V3	DIS2V5	PWRGD	FSEL1	FSEL2
PDO1 = 3V3ON	0	0	1	1	0	1	1	1	1
PDO2 = 2V5ON	0	0	0	1	0	0	1	1	1
PDO3 = Fault	0	0	0	0	1	1	0	1	1

Fig. 10

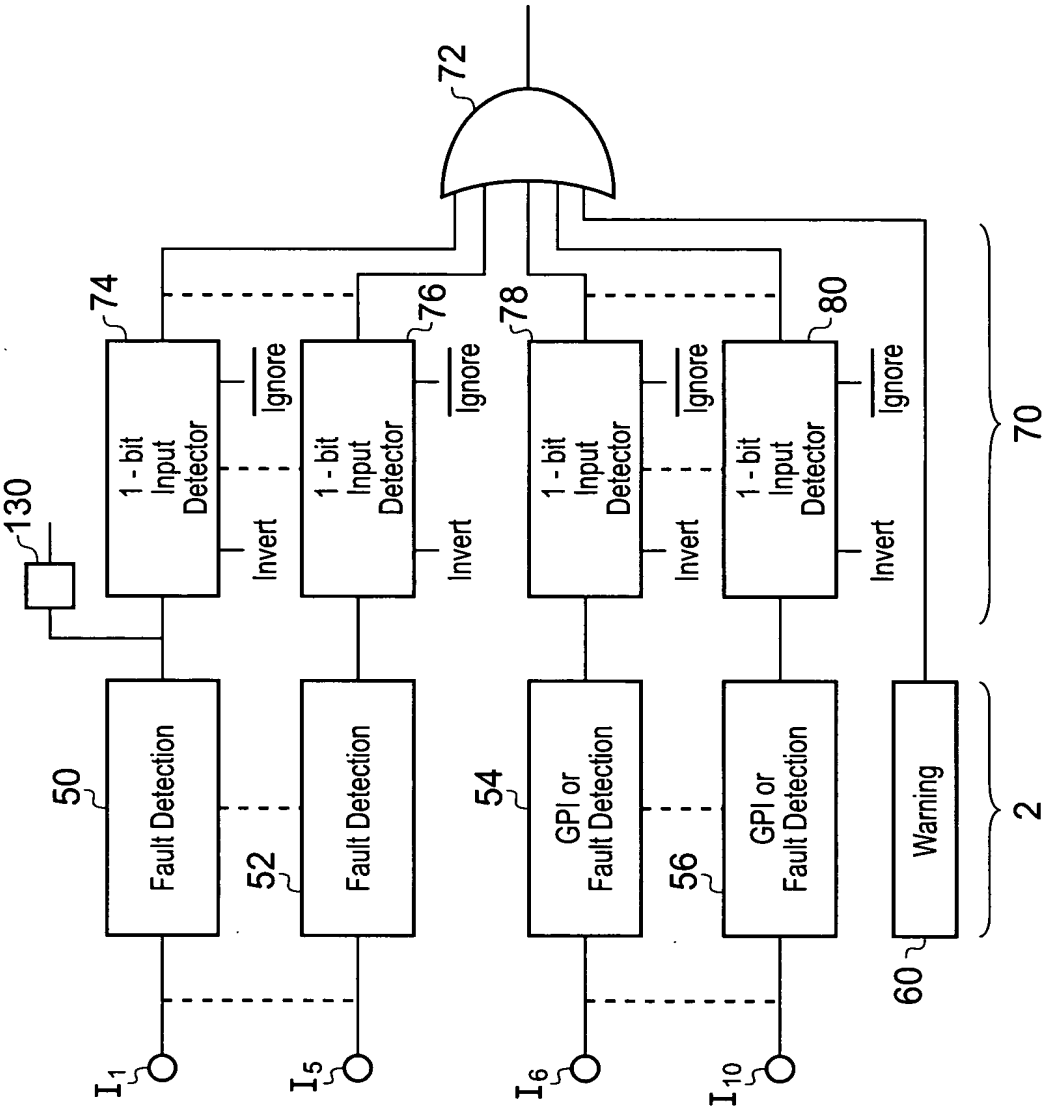
72
74
76
78
80
130
1 - bit Input Detector
Ignore
Invert
70
50
52
54
56
60
Fault Detection
GPI or Fault Detection
Warning
2
I_1
I_5
I_6
I_{10}

Fig. 3

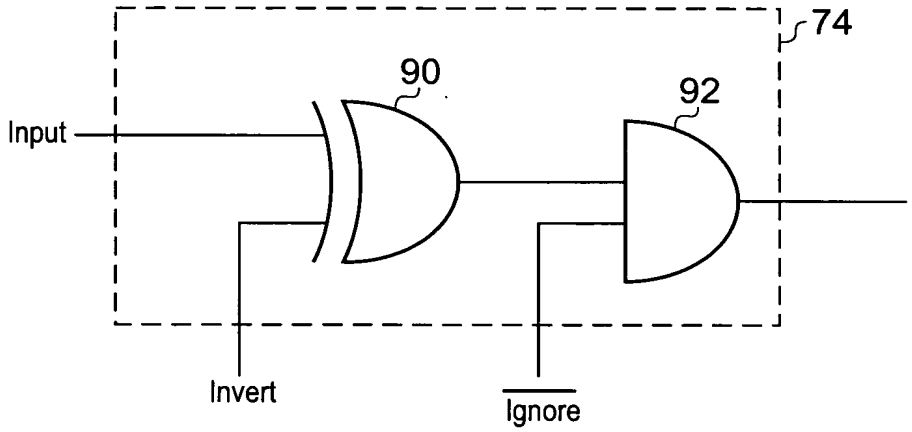

Fig. 4

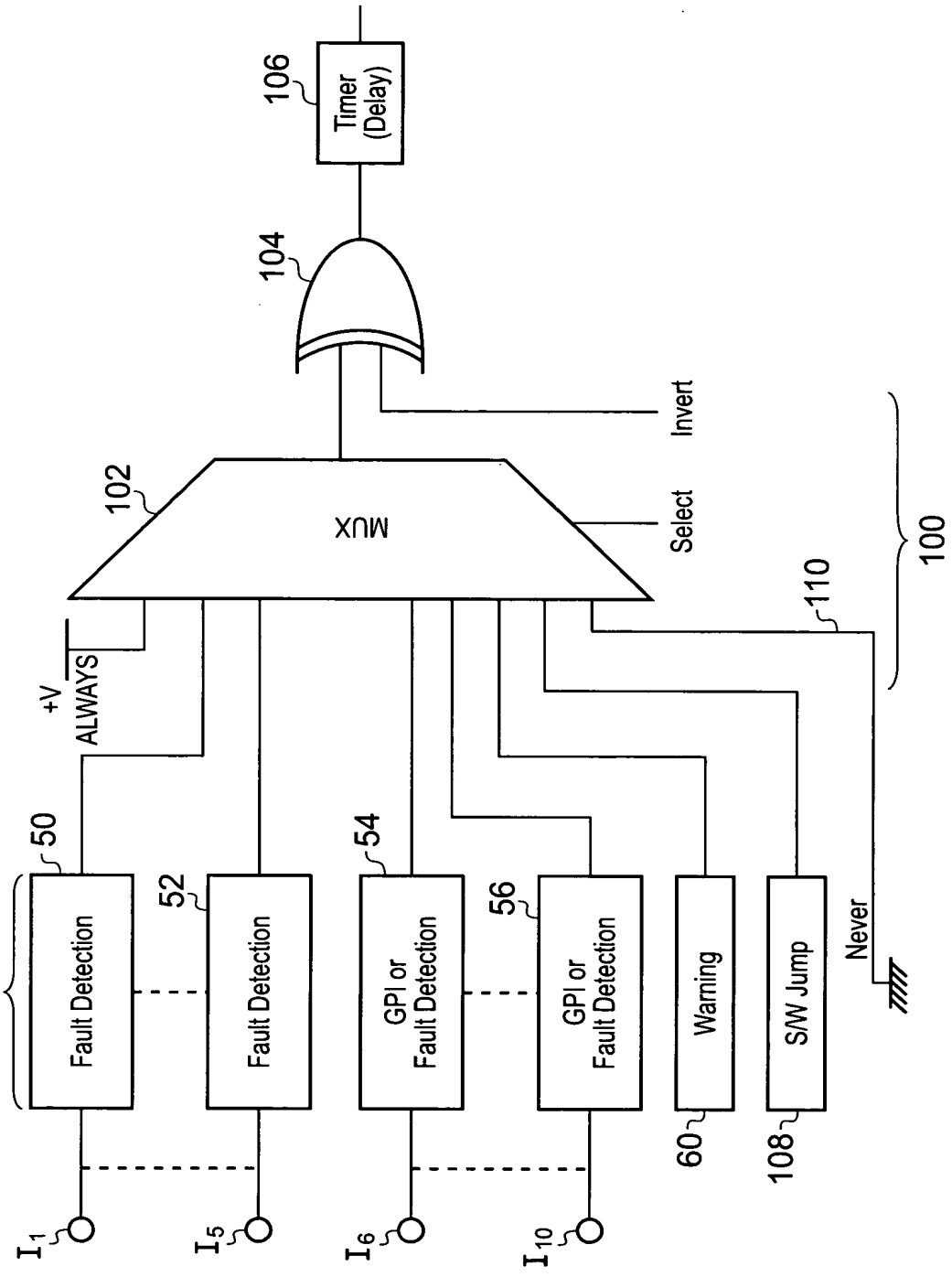
106
Timer (Delay)
104
Invert
102
MUX
Select
100
110
+V ALWAYS
50
52
54
56
2
Fault Detection
Fault Detection
GPI or Fault Detection
GPI or Fault Detection
Warning
S/W Jump
Never
60
108
I1
I5
I6
I10

Fig. 5

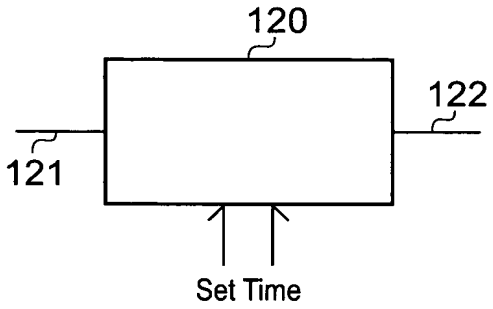
120
122
121
Set Time

Fig. 6

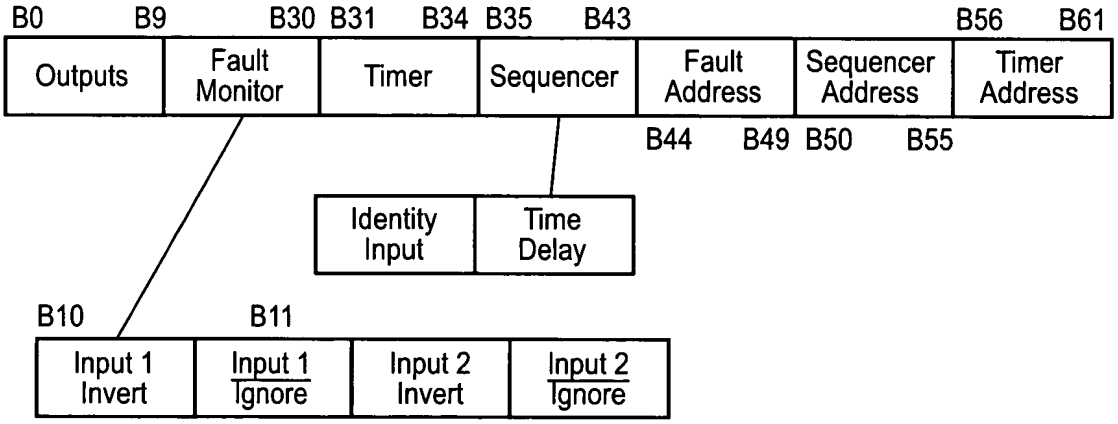
B0
B9
B30
B31
B34
B35
B43
B56
B61
Outputs
Fault Monitor
Timer
Sequencer
Fault Address
Sequencer Address
Timer Address
B44
B49
B50
B55
Identity Input
Time Delay
B10
B11
Input 1 Invert
Input 1 Ignore
Input 2 Invert
Input 2 Ignore

Fig. 7

State	End of Step	Timeout	Monitor
IDLE1	If VX1 is LOW then goto State IDLE2		
IDLE2	If VP1 is OK then goto State EN3V3		
EN3V3	If VP2 is OK then goto State EN2V5	If VP2 is NOT OK after 10ms then goto State DIS3V3	If VP1 is NOT OK then goto State IDLE1
DIS3V3	If VX1 is HIGH then goto State IDLE1		
EN2V5	If VP3 is OK then goto State PWRGD	If VP3 is NOT OK after 20ms then goto State DIS2V5	If VP1 or VP2 is NOT OK then goto State FSEL2
DIS2V5	If VX1 is HIGH then goto State DIS3V3		
FSEL1	If VP3 is NOT OK then goto State DIS2V5		If VP1 or VP2 is NOT OK then goto State FSEL2
FSEL2	If VP2 is NOT OK then goto State DIS3V3		If VP1 is NOT OK then goto State IDLE1
PWRGD	If VX1 is HIGH then goto State DIS2V5		If VP1 or VP2 or VP3 is NOT OK then goto State FSEL1

Fig. 8

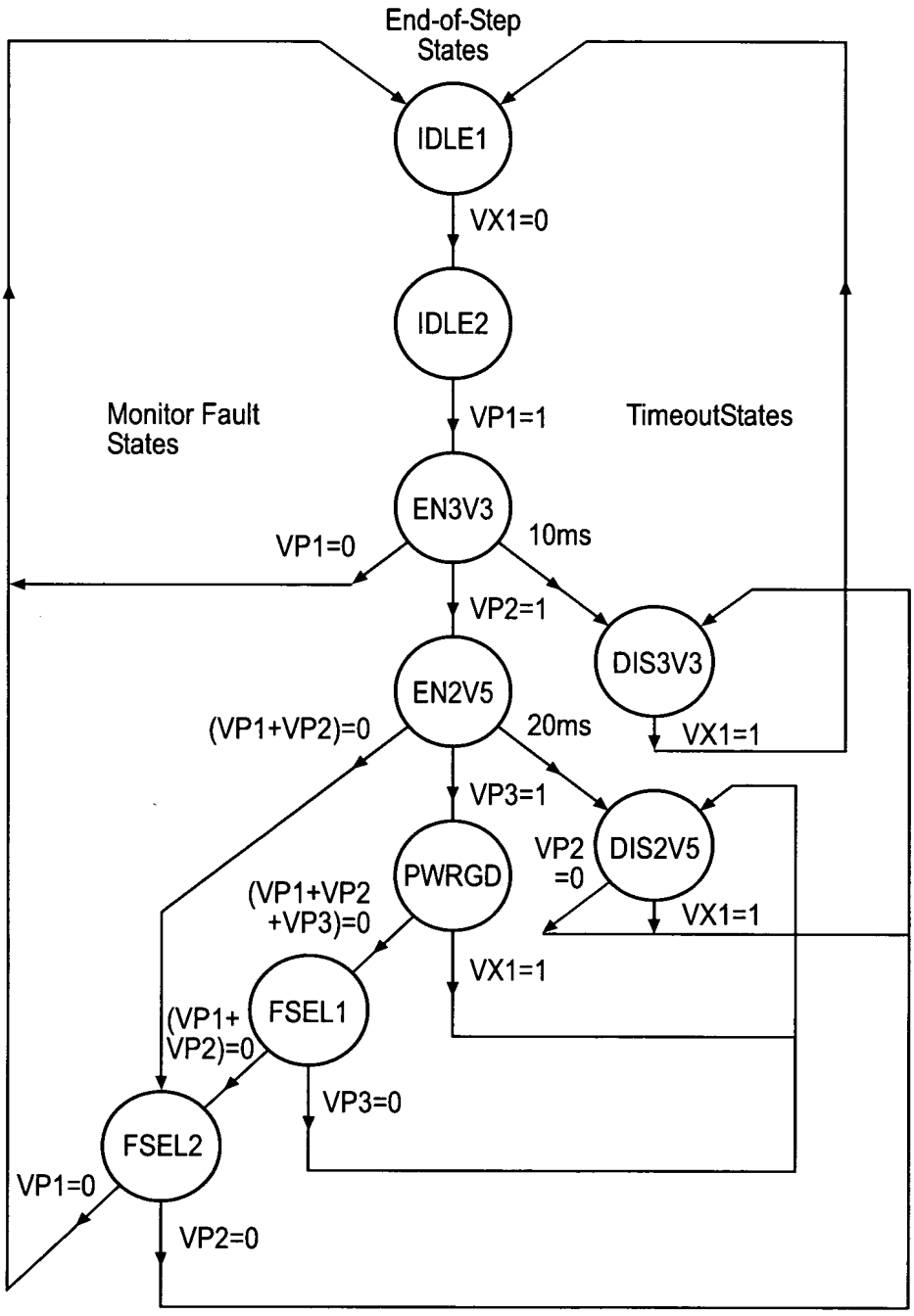
End-of-Step States
IDLE1
VX1=0
IDLE2
Monitor Fault States
VP1=1
TimeoutStates
EN3V3
VP1=0
10ms
VP2=1
DIS3V3
EN2V5
(VP1+VP2)=0
20ms
VX1=1
VP3=1
DIS2V5
VP2 =0
PWRGD
(VP1+VP2 +VP3)=0
VX1=1
VX1=1
FSEL1
(VP1+ VP2)=0
VP3=0
FSEL2
VP1=0
VP2=0

Fig. 9